COURSE DESCRIPTION CARD - SYLLABUS

Course name
Synchronous Digital Hierarchy in communication networks

Course

Field of study
Electronics and Telecommunications
Area of study (specialization)

Year/Semester
III/VI
Profile of study

Level of study
First-cycle studies
Form of study
full-time

Course offered in
English
Requirements
elective

Number of hours

Lecture
15
Laboratory classes
0
Other (e.g. online)

Tutorials
0
Projects/seminars
15

Number of credit points

3

Lecturers

Responsible for the course/lecturer:
dr hab. inż. Mieczysław Jessa

mieczyslaw.jessa@put.poznan.pl

Responsible for the course/lecturer:

Prerequisites

Student knows the principle of operation of digital transmission systems, digital modulations, forming the spectral properties of signals, countering channel distortions. Is able to extract information from Polish or English language literature, databases and other sources, is able to synthesize gathered information, draw conclusions, and justify opinions.

Course objective

The presentation of properties of basic transmission system exploited in modern communication networks and to create skills to assess utility of different transmission systems in real networks.

Course-related learning outcomes

Knowledge

1. Has a wide, systematic knowledge, with necessary mathematical background, of digital transmission systems and signal transmission methods.

Skills

1. Is able to assess basic parameters and properties of transmission systems used in real networks.

2. Is able to select adequate methods to solve typical tasks related to analysis, design and optimization of transmission systems.

Social competences

1. Is aware of the limitations of his/her current knowledge and skills; is committed to lifelong learning.

2. Is aware of the necessity to approach solving technical problems with responsibility and professionalism.

Methods for verifying learning outcomes and assessment criteria

Learning outcomes presented above are verified as follows:

Learning outcomes are verified with written/oral exam. Exam consists of 5 open questions. Answers are scored equally. Minimum number of scores to pass the exam is equal to 50%. Knowledge and skills gathered during the Project are assessed by written project and oral presentation of the results of this project. The final mark is the average of two marks. The assessment levels are the following: under 3 - mark 2,0, from 3 to 3, 25 - mark 3,0; from 3,26 to 3,75 - mark 3,5; from 3,76 to 4,25 - mark 4,0; from 4,26 to 4,75 - mark 4,5; above 4,75 - mark 5,0

Programme content

During the course students learn about basic transmission system used for data transmission between nodes of contemporary communication networks, called Synchronous Digital Hierarchy (SDH), and about its newer version, better adopted to data transmission coming from IP network, called Next-Generation SDH (NG-SDG). Program content includes: history of SDH, introduction to SDH, the layer concept, SDH network model, synchronous transport module, overheads structure, synchronous multiplexing, pointer justifications, virtual containers, tributary signals, SDH multiplexers (Terminal Multiplexer, Line Multiplexer, Add and Drop Multiplexer, Digital Crossconnect, Regenerator), SDH networks, uni- and bi-directional rings, mesh network, protection in SDH, connections of ring subnetworks, mapping of tributary signals to SDH, NG-SDH, virtual concatenation V-CAT, Link Capacity Adjustment Scheme (LCAS), and Generic Framing Procedure (GFC) used in NG-SDH.

The goal of the Project is to prepare and implement in software/hardware element or elements of SDH or NG-SDH. Students can choose subject from early prepared teacher's propositions or can propose its

own subject, after earlier acceptance of the teacher. Among existing propositions are: multiplexers of SDH; multiplexing four STM-1 signals into one STM-4; a circuit/software for BER assessment in RSOH or MSOH or VC-4, or VC-12; phase detector for wander and jitter measurements; computer model of synchronous multiplexing of four AU-4 into a single AU-4-4; computer model of asynchronous mapping of E1 into C-12; software/hardware model of error detection with BIP-K code, where K can assume 2, 8 or 16; header generator for STM-1 frame.

Teaching methods

Multimedia presentation and project method.

Bibliography

Basic

1. R. K. Jain „Principles of Synchronous Digital Hierarchy", CRC Press, Boca Raton, 2013.

Additional

1. A. Valdar „Understanding Telecommunications Networks", IET, London, 2006.

Breakdown of average student's workload

	Hours	ECTS
Total workload	75	3,0
Classes requiring direct contact with the teacher	40	2,0
Student's own work (literature studies, preparation for laboratory classes/tutorials, preparation for tests/exam, project preparation) [1]	35	1

[1] delete or add other activities as appropriate